REMARKS/ARGUMENTS

Claims 1-20 are pending in the present application. Claims 1-6, 10-13, and 15-20 were withdrawn in a previous restriction requirement. Claims 17 and 18 have been cancelled and claims 21 and 22 have been added. Claims 7-9 and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Horiuchi (USPN 4,960,365). Claim 14 is rejected under 35 U.S.C. § 102(b) as being anticipated by or on the alternative under 35 U.S.C. § 103(a) as being obvious over Horiuchi as evidenced by Takahashi et al (USPN 6,648,014). Applicant respectfully disagrees with the findings of the office action and argues the following:

Claims 7-9 and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Horiuchi. Applicant asserts that each and every limitation of amended claim 7 is not taught by Horiuchi and that this rejection has been overcome. Claim 7 has been amended to require in part "sending an output signal that is superimposed with a dither signal from the microprocessor to a pressure control." This amendment fins proper antecedent basis in the specification at page 4 lines 24-27.

Horiuchi does not teach sending an output signal that is superimposed with a dither signal from the microprocessor of the claim and instead teaches a command signal V_o that is received by a subtractor 6 that additionally receives a feedback signal V_f via swashplate 74 in order to provide a deviation signal V_e (Col. 13, lines 48-65). The deviation signal V_e is then outputted to a compensation circuit 14 to create a compensated deviation signal V_e' that is sent to a second subtractor 6'. Later in the line an amplified signal V_{e1} is received within an adder 10. (Col. 13, lines 48-65). Within the adder 10 a dithered signal V_d is added to create V_{e2}. Thus, the dithered signal V_d is introduced at the adder 10 and is not introduced in the compensation circuit 14

that the office action suggests is the microprocessor of the system. Thus specifically, the compensation circuit 14 does not superimpose a dither signal with an output signal to send to a pressure control as amended claim 7 requires and thus anticipation is not present. Consequently, Applicant respectfully requests the anticipation rejection be withdrawn.

Applicant also asserts that claim 7 is non obvious. Specifically, within the system taught by Horiuchi the dither V_d is only added to the amplified signal V_{e1} in the adder 10 in order to send to the comparator 8. The comparator 8 then pulse width modulates the signal V_{e2} in order to actuate the valve 80. (Col. 13, line 66-Col. 14, line 32). Therefore, the valve 80 does not receive a dithered output to provide an improved result as is taught by the present disclosure. Thus, Applicant asserts that the resolution and accuracy realized by Applicant's device is not shared by the device of Horiuchi. As a result, Applicant respectfully requests allowance of claim 7. Additionally, claims 8-9, 14 and new claims 21 and 22 depend on claim 7 and for at least for this reason are also considered allowable subject matter.

Applicant has added new dependent claims 21 and 22 and asserts that even if claim 7 is not considered allowable subject matter at the very least claims 21 and 22 present allowable subject matter. Claim 21 requires in part "the method of claim 7 further comprising the step of receiving a feedback signal within the microprocessor that is dependent on an angle of the swashplate." This amendment find proper antecedent basis in the specification at page 4 lines 1-5. The compensation circuit 14 that has been identified as the microprocessor does not receive a feedback signal that is dependent upon the swashplate and instead the subtractor 6 receives such a feedback signal. Thus,

Applicant asserts that Horiuchi does not anticipate dependent claim 21.

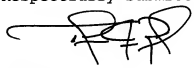
Dependent claim 22 requires "the method of claim 21 wherein the feedback signal and set point signal are averaged by the microprocessor." This claim gains proper antecedent basis in the specification at page 4, lines 2-14. Horiuchi teaches that the compensation circuit 14 compensates the deviation signal V_e thus outputting a compensated deviation signal V_e' to the subtractor 6'. (Col. 13, lines 55-58). Thus, Applicant asserts that claim 22 is not anticipated by the Horiuchi reference. Specifically, regarding claims 21 and 22 the microprocessor of the claimed device provides several functions including receiving a feedback signal, receiving the electric signal based on the set point signal, and superimposing an output signal with a dither signal. Applicant asserts that the Horiuchi reference does not teach a device that can be considered a microprocessor that receives all the signals contemplated by the claims and at the same time is able to generate or send output signals superimposed with a dither signal. As a result, a new and non obvious method is provided and Applicant respectfully requests allowance of all pending claims.

CONCLUSION

If any issues remain that may be expeditiously addressed in a telephone interview, the Examiner is encouraged to telephone the undersigned at 515/558-0200.

All fees or extensions of time believed to be due in connection with this response are attached hereto; however, consider this a request for any extension inadvertently omitted, and charge any additional fees to Deposit Account 50-2098.

Respectfully submitted,



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